



STMicroelectronics to advance next-generation chip manufacturing technology with new PLP pilot line in Tours, France

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- **Multi-disciplinary team to further develop innovative approach to chip packaging and test manufacturing technology boosting efficiency and flexibility**
- **Part of ST's strategic initiative on heterogeneous integration, contributing to technology roadmap on RF, analog, power and digital products**
- **Launch of the PLP pilot line in Tours supported by \$60 million investment and synergies with local R&D ecosystem**

Geneva, Switzerland, September 17, 2025 -- STMicroelectronics (NYSE: STM), a global semiconductor leader serving customers across the spectrum of electronics applications, today announced new details regarding the development of the next generations of Panel-Level Packaging (PLP) technology through a pilot line in its Tours site, France, which is expected to be operational in Q3 2026.

PLP is an advanced, automated chip packaging and test process technology bringing increased manufacturing efficiency and reducing costs, and a key enabler for creating the next generation of smaller, more powerful, and cost-effective electronic devices. The large-area carrier in PLP (large rectangular shapes in place of circular wafers) enables higher manufacturing throughput, making it a more efficient solution for high-volume production. Building on its first-generation PLP line in operation in Malaysia and its global technology R&D network, ST plans to develop the next generations of its PLP technology to maintain its technological leadership and extend the use of PLP across many other ST products for automotive, industrial and consumer applications.

"The development of our PLP capabilities in our Tours site is aimed at advancing this innovative approach to chip packaging and test manufacturing technology, boosting efficiency and flexibility so it can be rolled out across a wide portfolio of applications, including RF, analog, power and microcontrollers. A multidisciplinary team of experts in manufacturing automation, process engineering, data science and analytics, as well as technology and product R&D, will collaborate on this program, which is a key part of a larger strategic initiative focused on heterogeneous integration – a scalable, efficient new approach to chip integration," said Fabio Gualandris, President Quality, Manufacturing and Technology of STMicroelectronics. *"With our fab in Malta, ST has already demonstrated its capability to deliver high-performing chip packaging and test in Europe. As we reshape our global manufacturing footprint, this new initiative in Tours will expand our process, design and manufacturing innovation capabilities supporting the development of next-generation chips in Europe".*

The development of the new PLP pilot line in Tours is supported by a capital investment of over \$60 million, already allocated as part of the company-wide program to reshape the Company's manufacturing footprint. Additional synergies are expected with the local R&D ecosystem, including the CERTEM R&D center. As previously announced, this program is focused on advanced manufacturing infrastructure and brings redefined missions for some sites in France and Italy to support their long-term success.

Technical note on PLP

For decades, the industry has relied on wafer-level packaging (WLP) and flip-chip technology to connect silicon chips to external circuitry. However, as devices become smaller and more complex, these methods have begun to reach their limits in terms of scalability and cost-effectiveness. For advanced packaging, different approaches exist or are under development; PLP is one of them.

Panel Level Packaging is a method where multiple ICs are packaged on a single, larger rectangular substrate panel, rather than on individual circular wafers. This allows for more ICs to be processed simultaneously, reducing costs and improving throughput.

ST has not only adopted PLP-DCI but has also been at the forefront of its development since 2020. The company's research and development teams have worked to prototype and scale the technology, culminating in a state-of-the-art PLP-DCI process currently in production at very high volumes of over 5 million units per day on a highly automated line using very large, 700x700mm panels.

STs PLP technology focuses on Direct Copper Interconnect (DCI). Direct copper interconnections replace the traditional wire

connections of chips with their encapsulation support. DCI is the process by which these ICs are electrically connected to the panel substrate using copper, which is known for its excellent electrical conductivity. DCI offers superior performance compared to traditional methods that use solder bumps, which can be less reliable. This technology with direct connection without wire supports new product development by reducing power losses (such as resistance and inductance), enhancing heat dissipation and enabling miniaturization. This leads to better overall power density.

PLP-DCI also allows the integration of multiple chips within advanced packages, known as System in Package (SiP).

About STMicroelectronics

At ST, we are 50,000 creators and makers of semiconductor technologies mastering the semiconductor supply chain with state-of-the-art manufacturing facilities. An integrated device manufacturer, we work with more than 200,000 customers and thousands of partners to design and build products, solutions, and ecosystems that address their challenges and opportunities, and the need to support a more sustainable world. Our technologies enable smarter mobility, more efficient power and energy management, and the wide-scale deployment of cloud connected autonomous things. We are on track to be carbon neutral in all direct and indirect emissions (scopes 1 and 2), product transportation, business travel, and employee commuting emissions (our scope 3 focus), and to achieve our 100% renewable electricity sourcing goal by the end of 2027. Further information can be found at www.st.com.

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Attachment

- [PLP Technology-Tours announcement -FINAL FOR PUBLICATION](#)