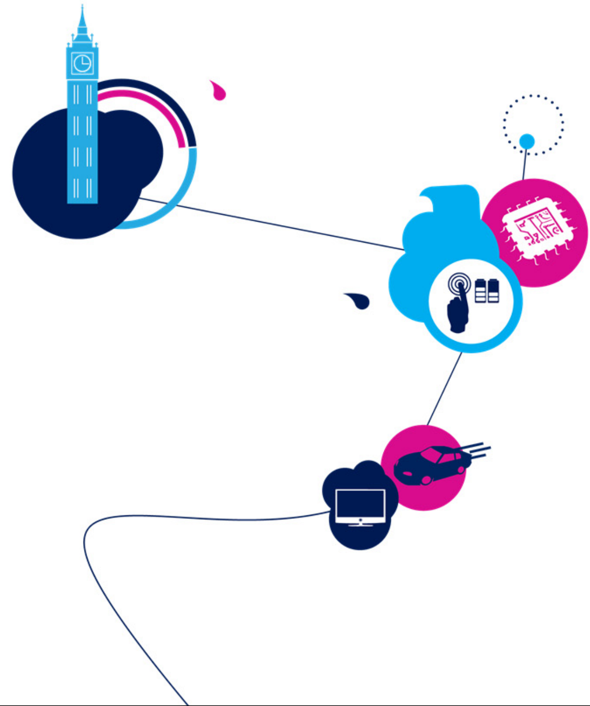
Technology R&D and Manufacturing

Jean-Marc Chery
Executive Vice President
Chief Manufacturing & Technology Officer,
General Manager, Digital Sector



Agenda

- Introduction
- Technology – Embedded Processing Solutions
- Technology – Sense & Power and Automotive
- Manufacturing
- Conclusion

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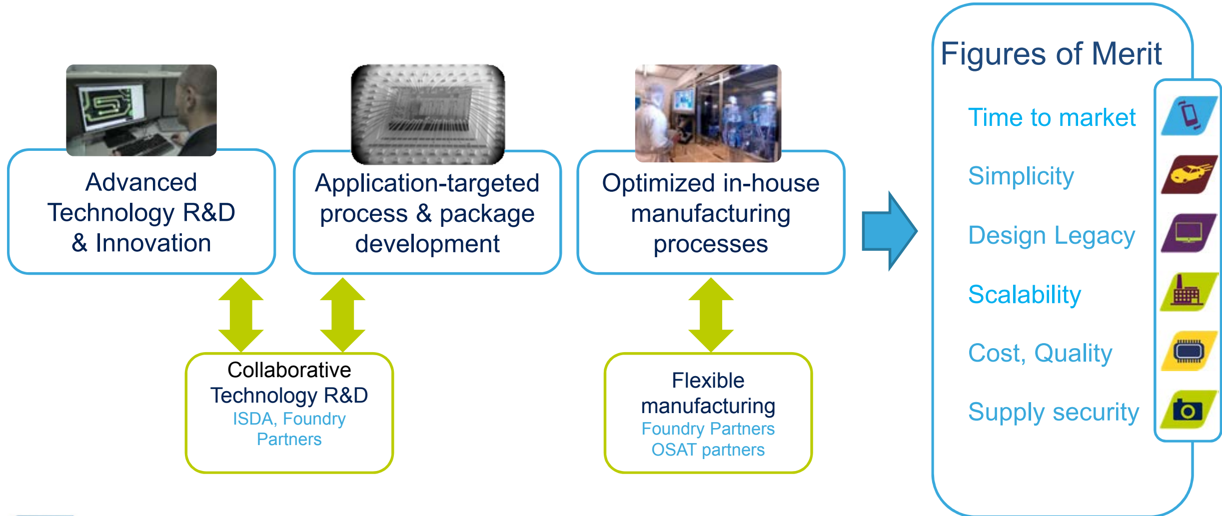
The Right Model for Our Industry



ISDA: International Semiconductor Development Alliance
OSAT: Outsourced Assembly and Test

Technology Portfolio Enabling Business

Sense & Power and Automotive Products

Analog, MEMS & Sensors

Automotive Products Group

Industrial & Power Discrete

Process

MEMS

Advanced CMOS FD-SOI

Analog Mixed Signal/RF

eNVM

Power & Discrete

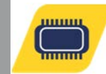
CMOS Image Sensor

BCD

BiCMOS

Packaging

Digital Convergence Group



Microcontrollers, Memory & Security

Imaging, BiCMOS ASIC & Silicon Photonics

Embedded Processing Solutions

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EPS - Technology Roadmap

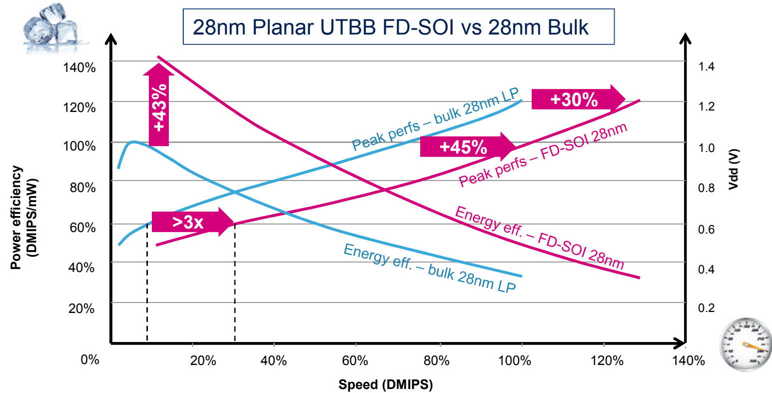
Prototyping start	2013	2014/15	2016/17
CMOS Digital (including RF)	28nm UTBB FD-SOI	14nm UTBB FD-SOI	10nm UTBB FD-SOI

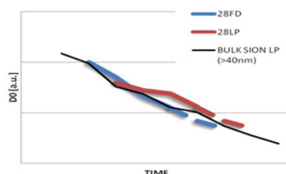
FD-SOI: Fully Depleted Silicon On Isolator
UTBB: Ultra Thin Body and BOX (Buried Oxide)

- Convergence to FinFET expected at 7nm
- FinFET know-how being developed in the framework of the ISDA Alliance

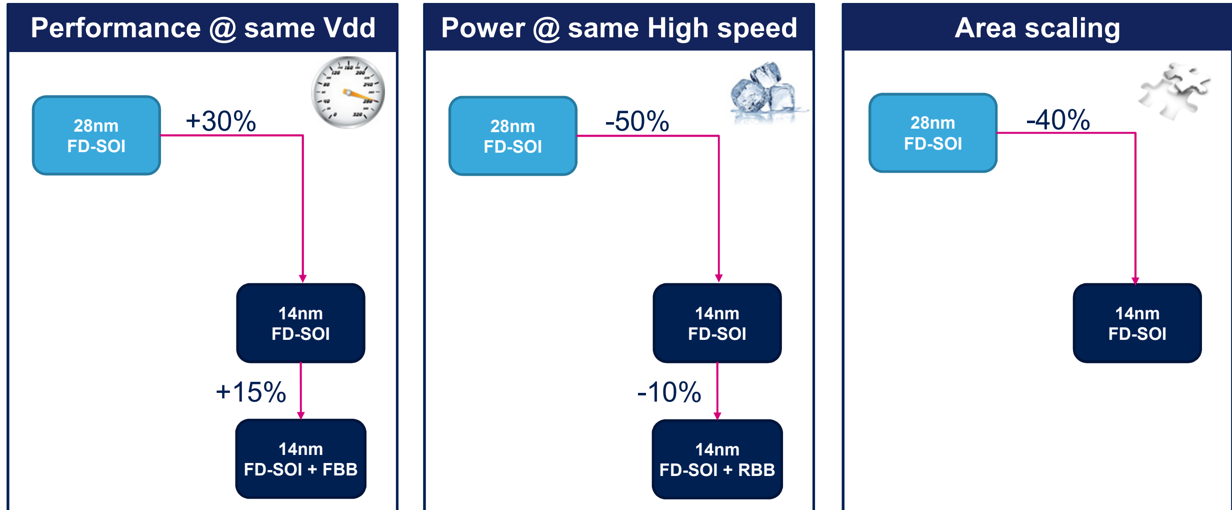
Best in Class Technology at 28nm

- Superior technology at 28nm delivering what customers want
- ST products based on FD-SOI have competitive advantage
- Winning ASIC business thanks to performance/power and simpler process than alternative
- Yield Learning Equivalent to Traditional Bulk Process





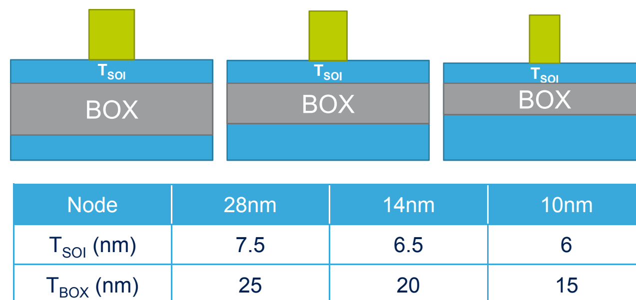
Continuing Technology Superiority at 14nm



FBB: Forward Body Bias

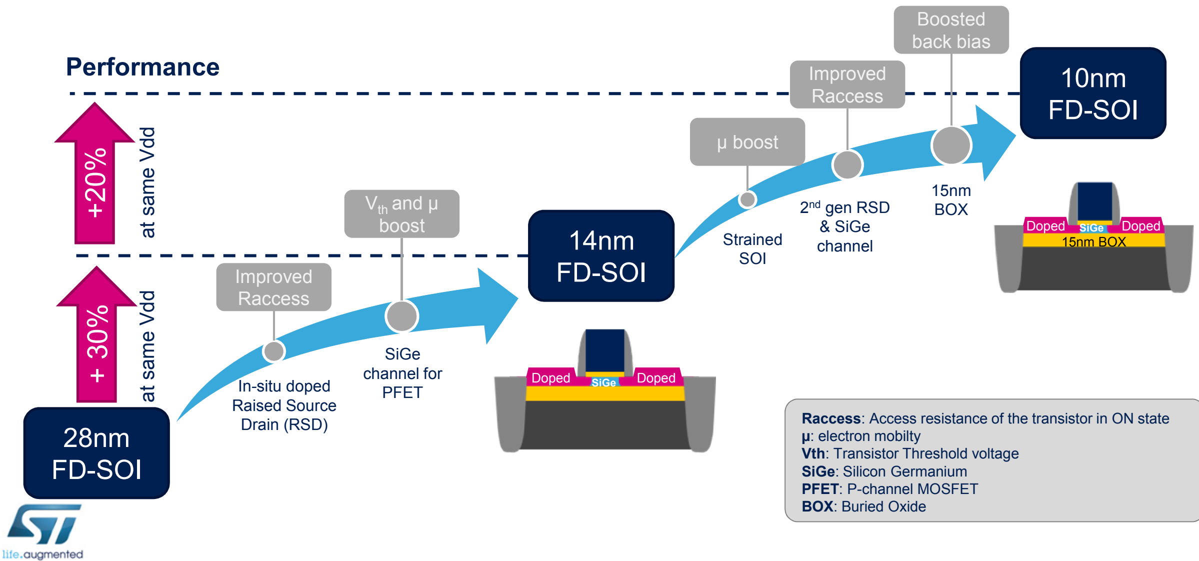
RBB: Reverse Body Bias

Planar UTBB FD-SOI : Scalability obtained by reduction of T_{SOI} & T_{BOX}



Node	28nm	14nm	10nm
T_{SOI} (nm)	7.5	6.5	6
T_{BOX} (nm)	25	20	15

- Electrostatic control improved by Thinning T_{BOX}
- Scalability down to 10nm node
- Devices already processed with 3.5nm SOI film


Planar UTBB FD-SOI Scalability
Boosters Roadmap
11
Performance
+20%
at same Vdd
+ 30%
at same Vdd
28nm
FD-SOI
Improved
Raccess
In-situ doped
Raised Source
Drain (RSD)
Vth and μ
boost
SiGe
channel for
PFET
14nm
FD-SOI
Doped
SiGe
Doped
μ boost
Strained
SOI
Improved
Raccess
2nd gen RSD
& SiGe
channel
Boosted
back bias
15nm
BOX
10nm
FD-SOI
15nm BOX
Raccess: Access resistance of the transistor in ON state
μ: electron mobilty
Vth: Transistor Threshold voltage
SiGe: Silicon Germanium
PFET: P-channel MOSFET
BOX: Buried Oxide
life.augmented

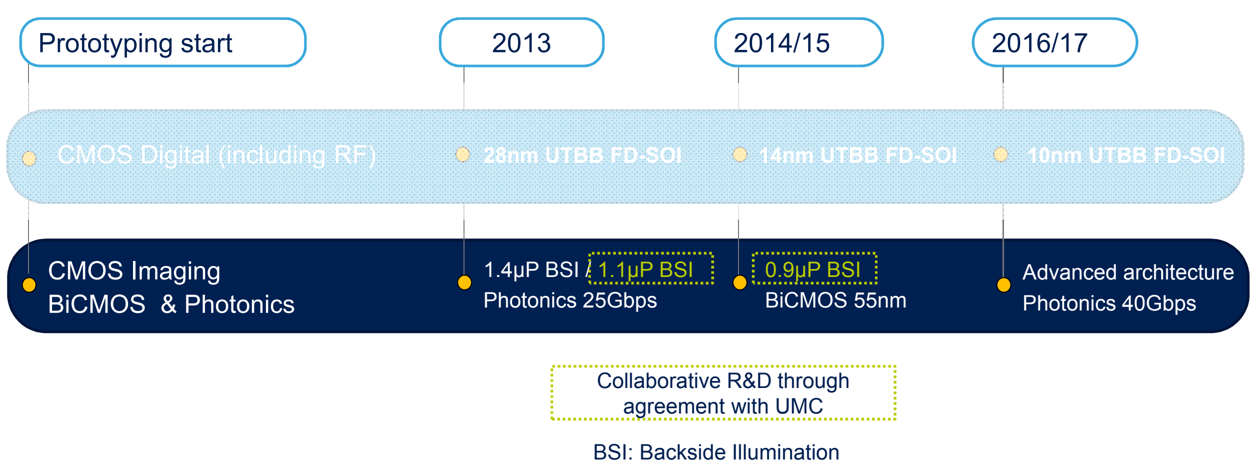
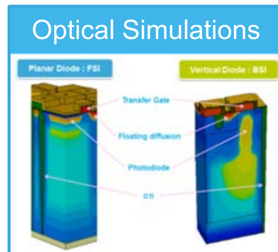

EPS - Technology Roadmap
12
Prototyping start
2013
2014/15
2016/17
CMOS Digital (including RF)
28nm UTBB FD-SOI
14nm UTBB FD-SOI
10nm UTBB FD-SOI
CMOS Imaging
BiCMOS & Photonics
1.4μP BSI / 1.1μP BSI
Photonics 25Gbps
0.9μP BSI
BiCMOS 55nm
Advanced architecture
Photonics 40Gbps
Collaborative R&D through
agreement with UMC
BSI: Backside Illumination
life.augmented

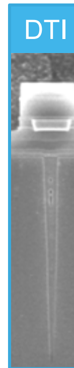
Image Sensors Differentiating Factors

Stitching

Optical Simulations

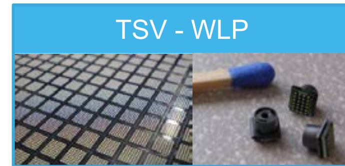


DTI



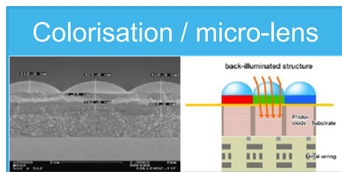
DTI:
Deep Trench Isolation

TSV - WLP

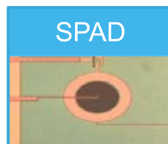


TSV: Though Silicon Via
WLP: Wafer-Level Package

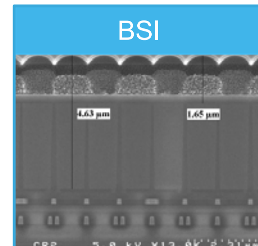
Colorisation / micro-lens



SPAD



BSI

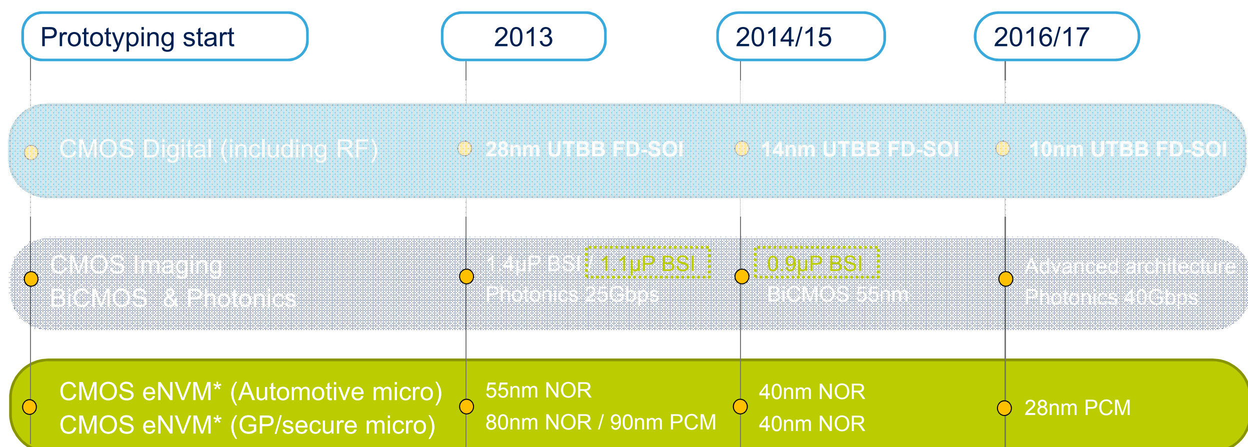


BSI: Backside Illumination

High Speed IOs

Optimized Design Solution

EPS - Technology Roadmap

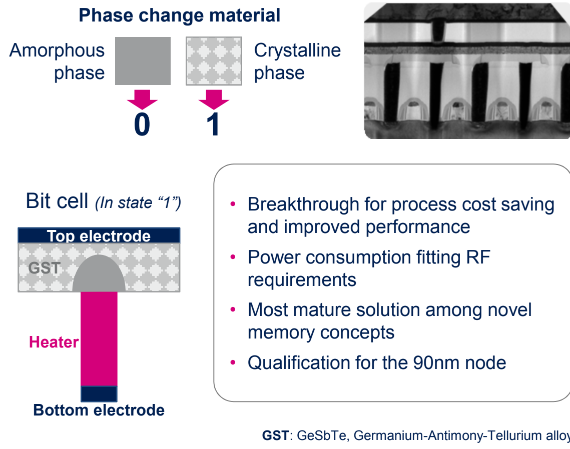


*Logic with embedded memories

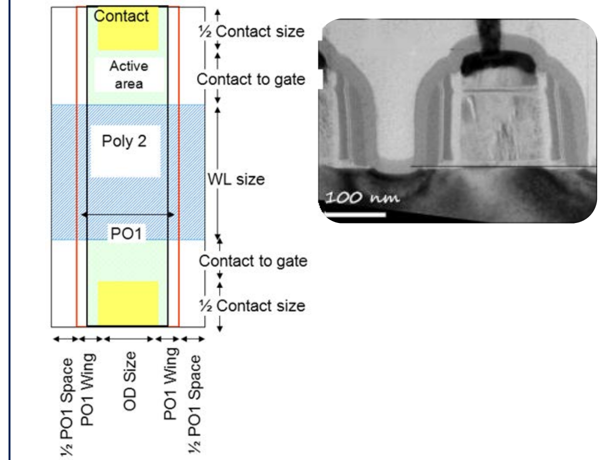
eNVM: embedded Non Volatile Memory
PCM: Phase Change Memories

Non-Volatile Memory Differentiators

Phase Change Memory (PCM) Technology



NOR 40nm eFlash



EPS - Technology Roadmap

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CMOS Digital (including RF)	**28nm UTBB FD-SOI**	**14nm UTBB FD-SOI**	**10nm UTBB FD-SOI**
CMOS Imaging BiCMOS & Photonics	1.4µP BSI / 1.1µP BSI Photonics 25Gbps	0.9µP BSI BiCMOS 55nm	Advanced architecture Photonics 40Gbps
CMOS eNVM* (Automotive micro) CMOS eNVM* (GP/secure micro)	55nm NOR 80nm NOR / 90nm PCM	40nm NOR 40nm NOR	28nm PCM

*Logic with embedded memories

FD-SOI: Fully Depleted Silicon On Isolator
UTBB: Ultra Thin Body and BOX (Buried Oxide)

Cooperative R&D through agreement with Foundry

BSI: Backside Illumination
eNVM: embedded Non Volatile Memory
PCM: Phase Change Memories

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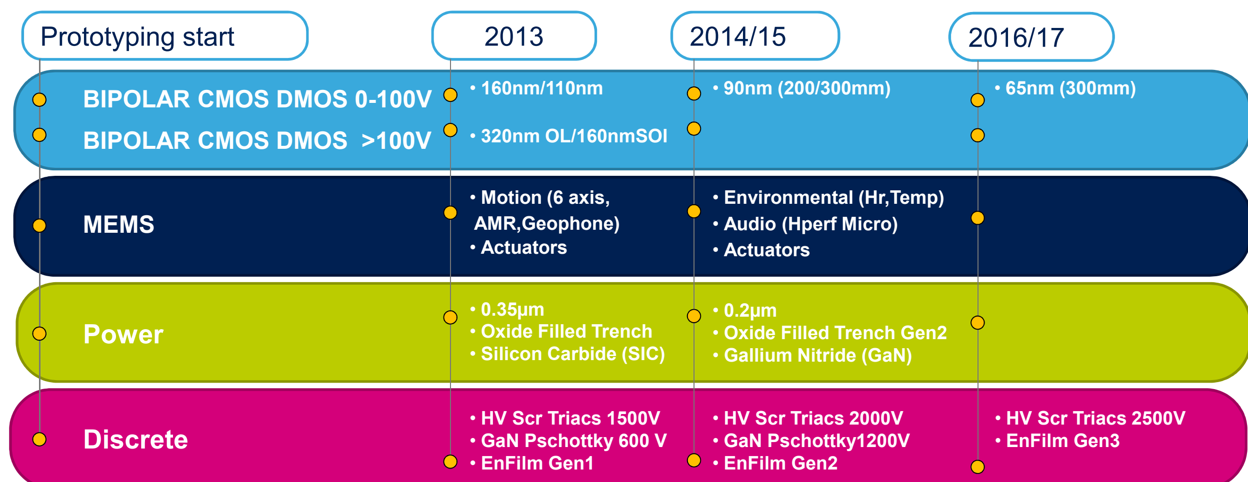
SPA - Technology Roadmap

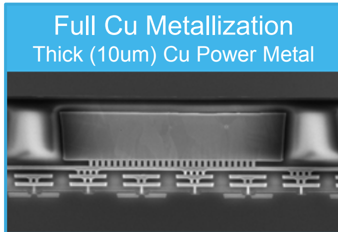


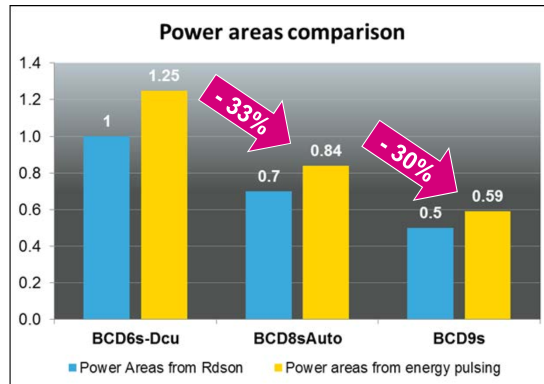
Smart Power: Leading with BCD9S

BCD9S

- 1.8V CMOS / 5V Analog
- 8V to 100V
- 130Kgates/mm2

Full Cu Metallization
Thick (10um) Cu Power Metal





Tier-1 automotive customer award for next generation braking system

All Technologies for MEMS

Silicon Technologies

- Moore's Law: Miniaturization
- More than Moore: Functionalities
- 3D Structure: i.e. MEMS
- Through-Silicon Vias

+

New Materials

- Getters
- Polymers
- Shape Memory Alloy
- Piezoelectric (PZT)
- SiC & GaN
- Graphene

+

Package

- Wafer Level Packaging (Stacked Multi Dice)
- New interconnections (Bondless, Sintering, Cu on Cu)
- Smart System In Package (SiP)

Technology and manufacturing for full spectrum of MEMS

MOTION MEMS

Accelerometers
Compass
Gyroscopes
Brain

MICRO-ACTUATORS

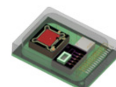
Electrostatic
Piezoelectric
Thermal

ACOUSTIC MEMS

Microphones
Loudspeakers

ENVIRONMENTAL MEMS

Pressure
Temperature
Humidity
Chemical
Infrared



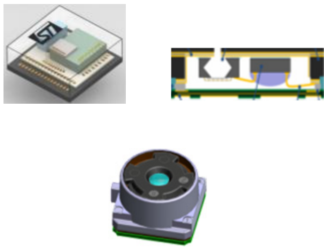
Packaging Technology R&D

Applicative | **Advanced**

Sense

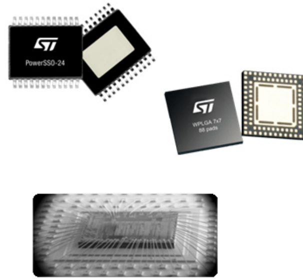
MEMS & microphones (LGAs)

Optical modules and Imagers towards BSI



Power & BCD

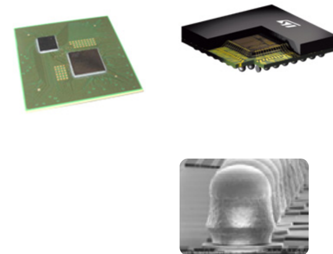
High dissipation, miniaturized packages (PSSO, QFNs)



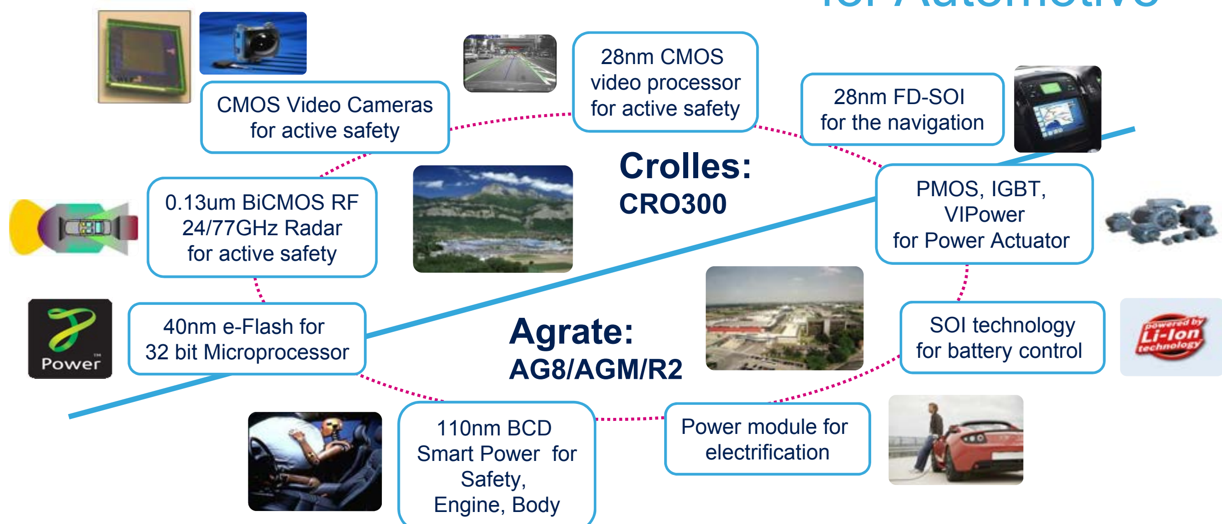
Digital with advanced CMOS

Integration and miniaturization based on BGAs.

Towards Flip Chip &WLP



Mastering all Technologies and Manufacturing for Automotive



Priorities for 2013 - Technology

2013

BCD9S technology platform to be ready for production
Power ASIC for Automotive (ABS/ESP) engineering samples delivery demonstrating superior device performances and die area reduction

FD-SOI 14 nm technology to be ready for prototyping and IPs validation vehicles for superior performances and low power consumption SoC and ASICs

Embedded flash 40nm technology for high performance MCUs
Readiness for prototyping and IPs validation vehicles

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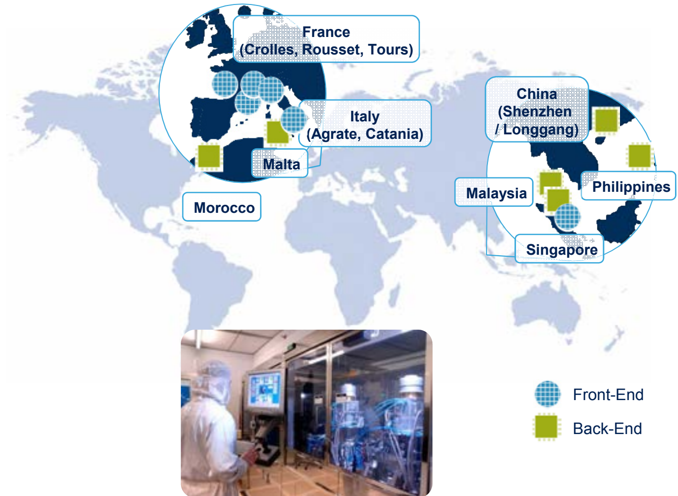
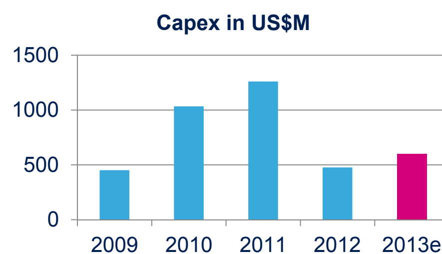
Manufacturing Model

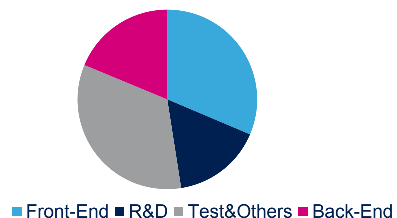
- Manufacturing model unchanged
  - Independent manufacturing
  - Supply flexibility provided by foundries
- Efficient manufacturing tool at about $2.2B-$2.3B quarter run rate
- 6 Front-end sites
  - 20% outsourcing target
- 6 Back-end plants
  - 30% outsourcing target



Manufacturing & Technology R&D CAPEX

- Proven ability to significantly modulate Capex
  - Essentially driven by decisions to add global capacity on top of technology mix evolution
- 2013 Capex expected to be approximately $550M-$600M
  - 300mm 14nm FD-SOI capability
  - 300mm Image Sensor BSI capacity
  - MEMS
  - Smart-Power mix change
  - Capacity increase & mix evolution in back-end
  - Copper wire conversion





Internal Manufacturing Advantage

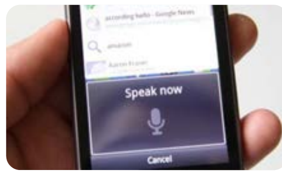
We win business thanks to the full control and flexibility in our supply chain

Digital

- Fastest prototyping service
- Fast ramp to volume

MEMS

- Fast ramp to volume
- Control of all the parts

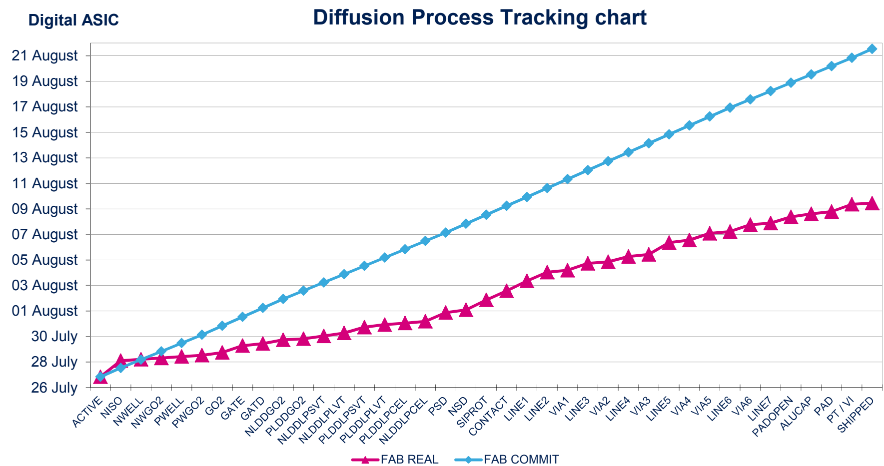


Automotive

- Customer requirement
- Quality & Reliability

Fastest Prototyping for Digital ASIC

Prototype shipped 13 days in advance of committed schedule with 0.37 days per mask layer



Priorities 2013 – Manufacturing

2013

300mm Crolles
- CMOS FD-SOI 28nm Manufacturing ramp-up
- Imaging 1.4µP BSI volume production

e-NVM and RF/Analog
- 90nm e-Flash high volume production
- Optimized130nm RF SOI in production ramp-up

Smart Power and Discrete
- BCD mix evolution to 0.16um / thick Cu
- IGBT 650/1200V production ramp-up

MEMS
- 6-Axis combo volume production
- µPhone and Compass production ramp-up

Innovation
Time to Volume
Quality Excellence
Lean Manufacturing
Productivity
Cost reduction